

Figure 1(a). Pipelined Memory Array

Figure 1(a)

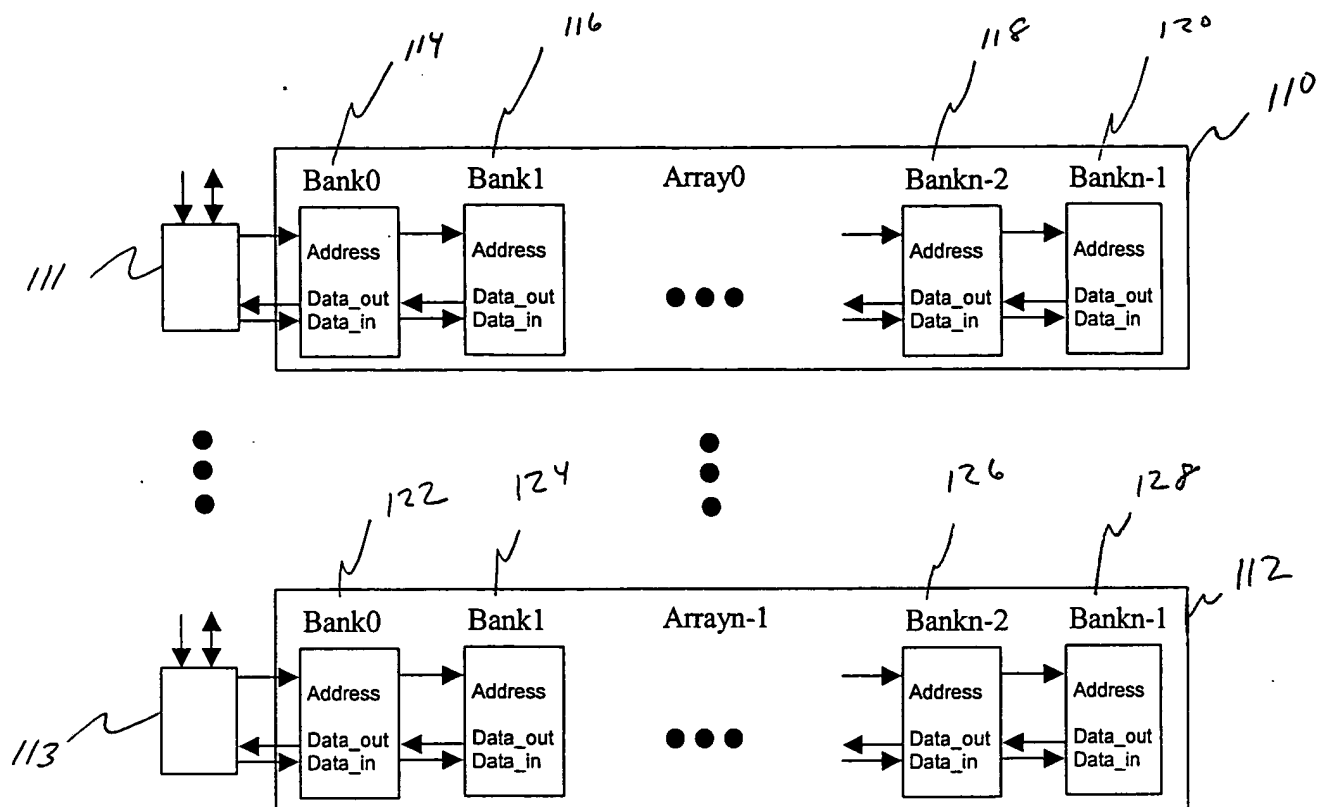


Figure 1(b). Systolic Memory Array

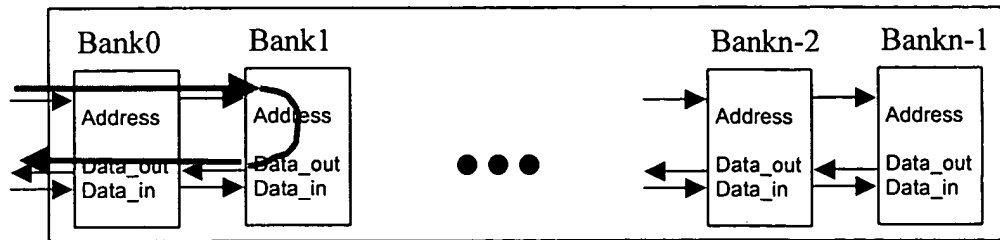


Figure 2(a) Read Address/Data Movement

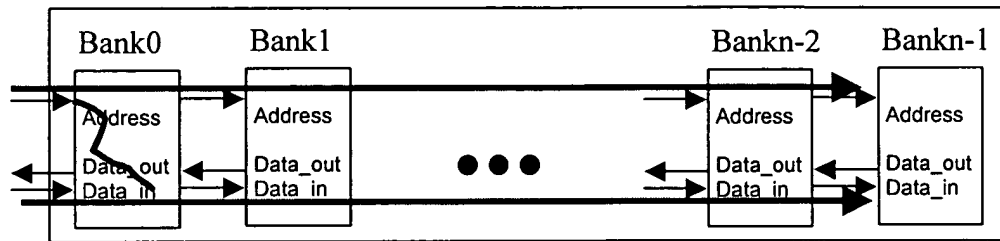
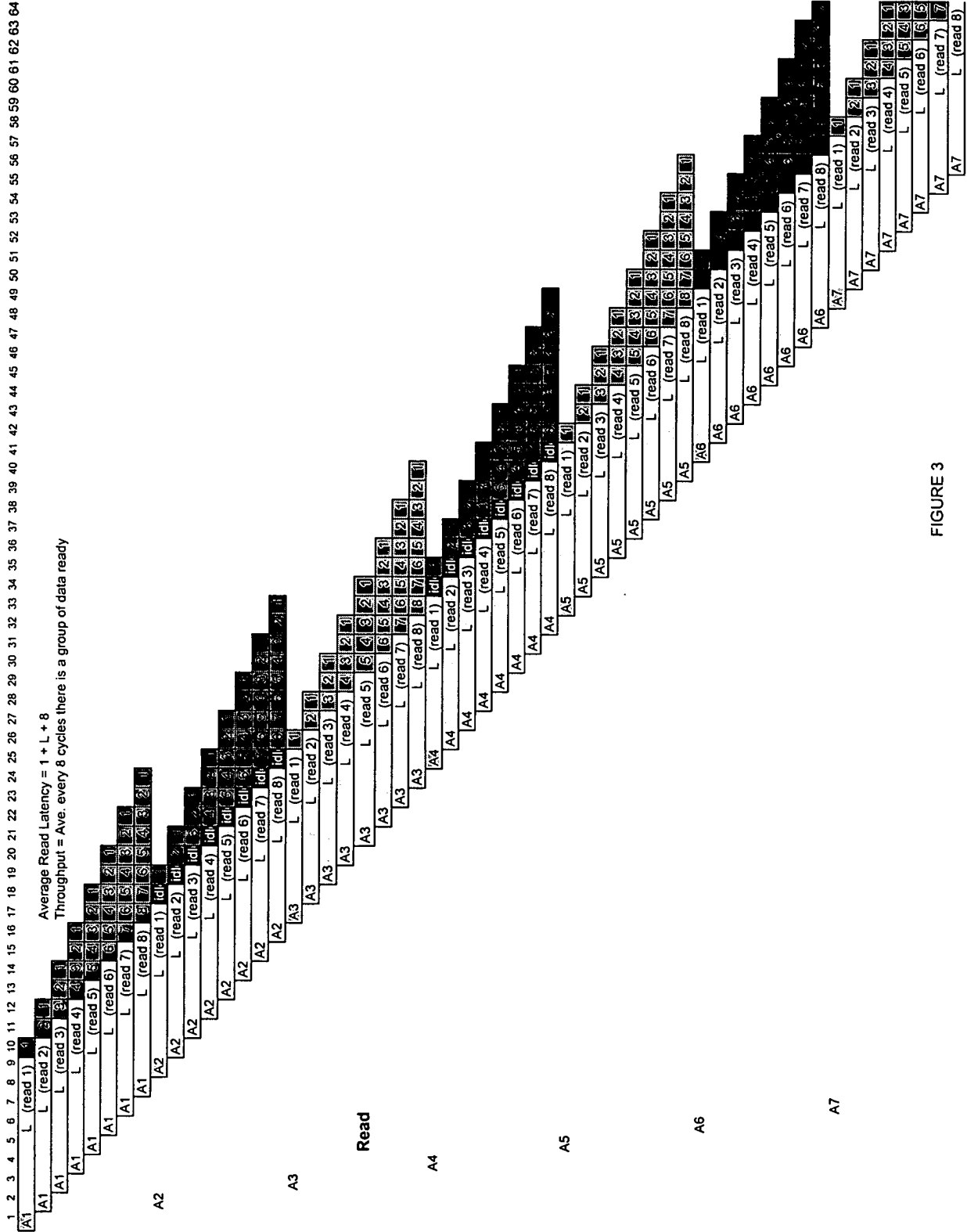
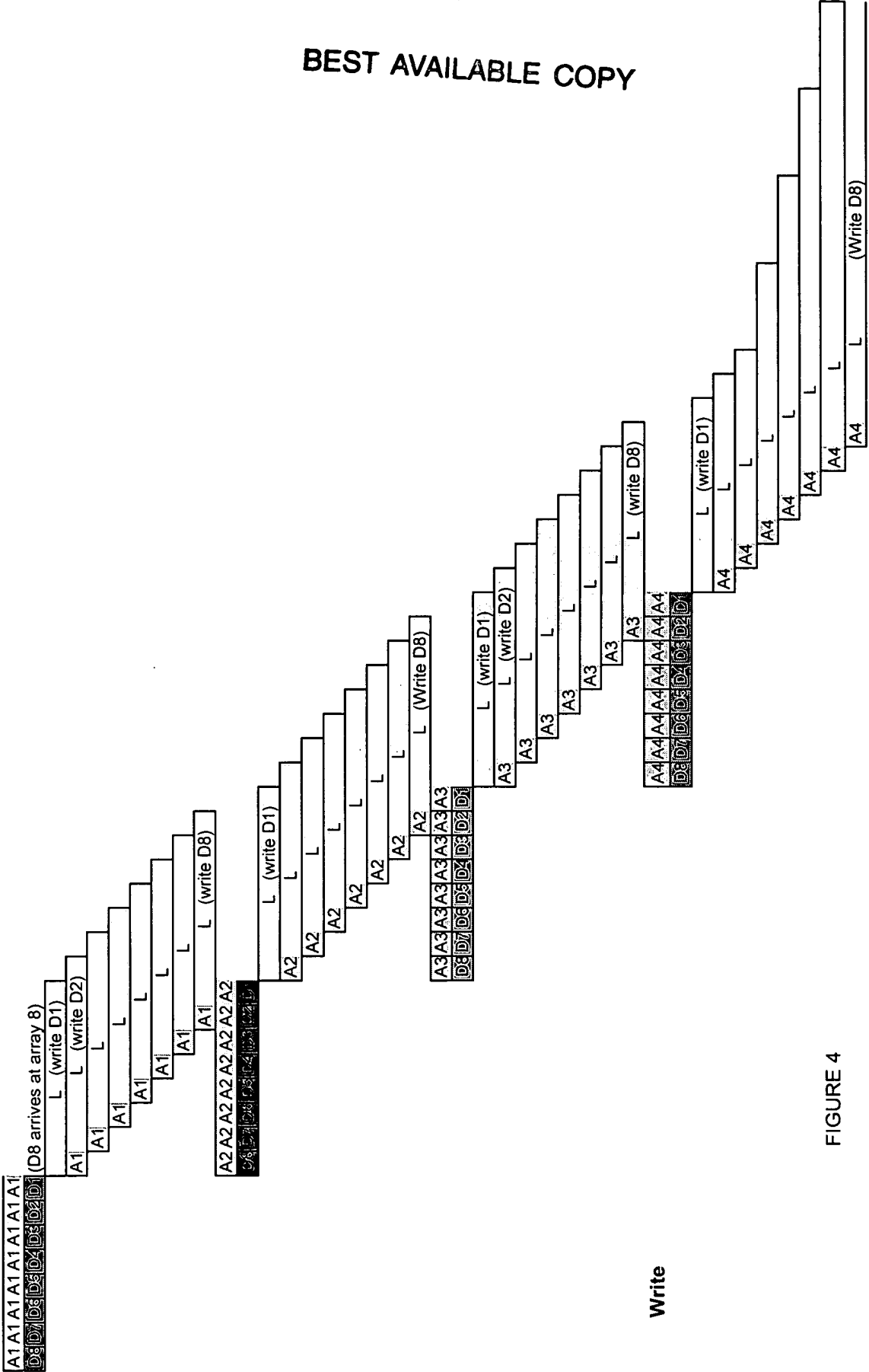


Figure 2(b) Write Address/Data Movement

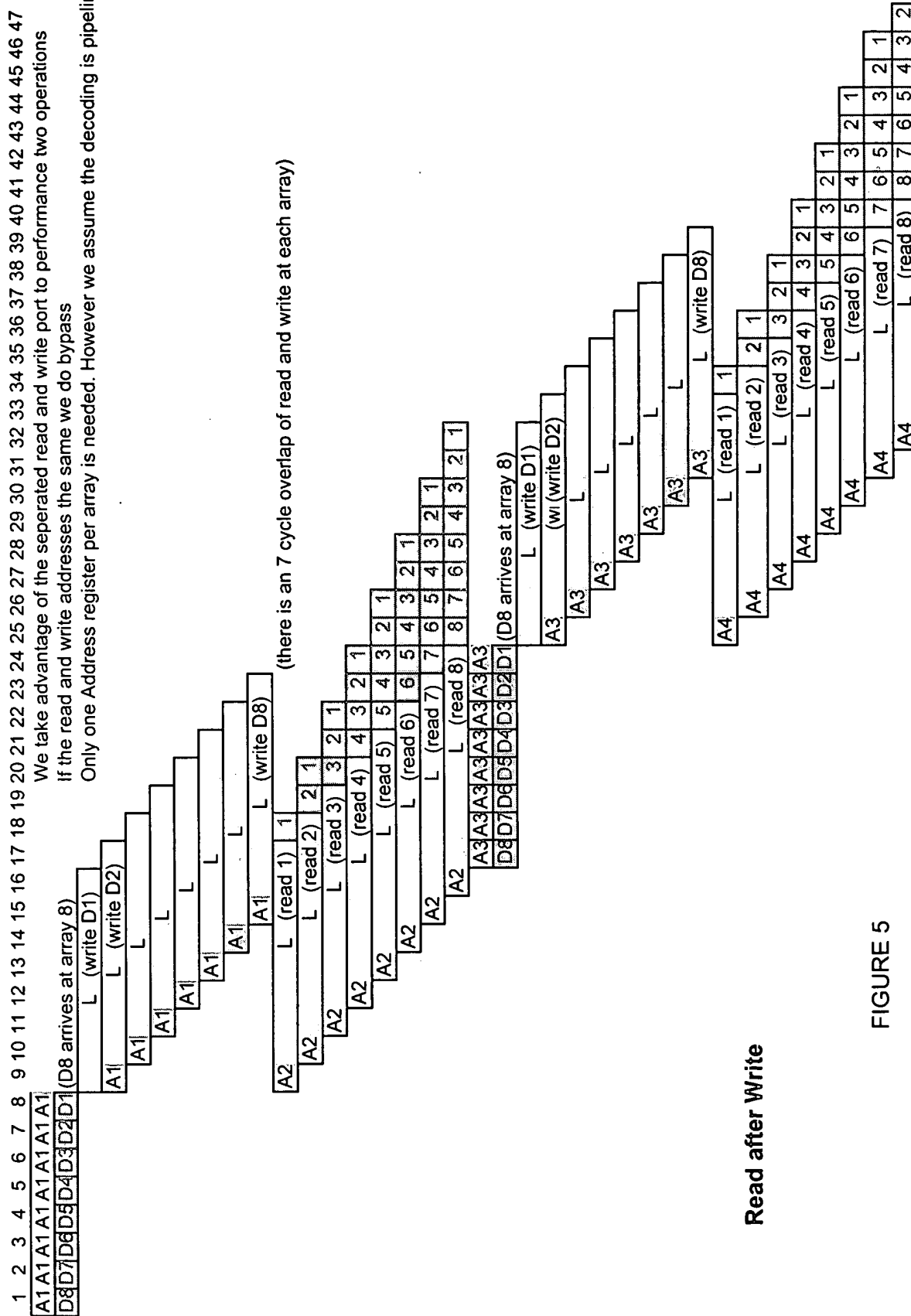
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FIGURE 4



[illegible]

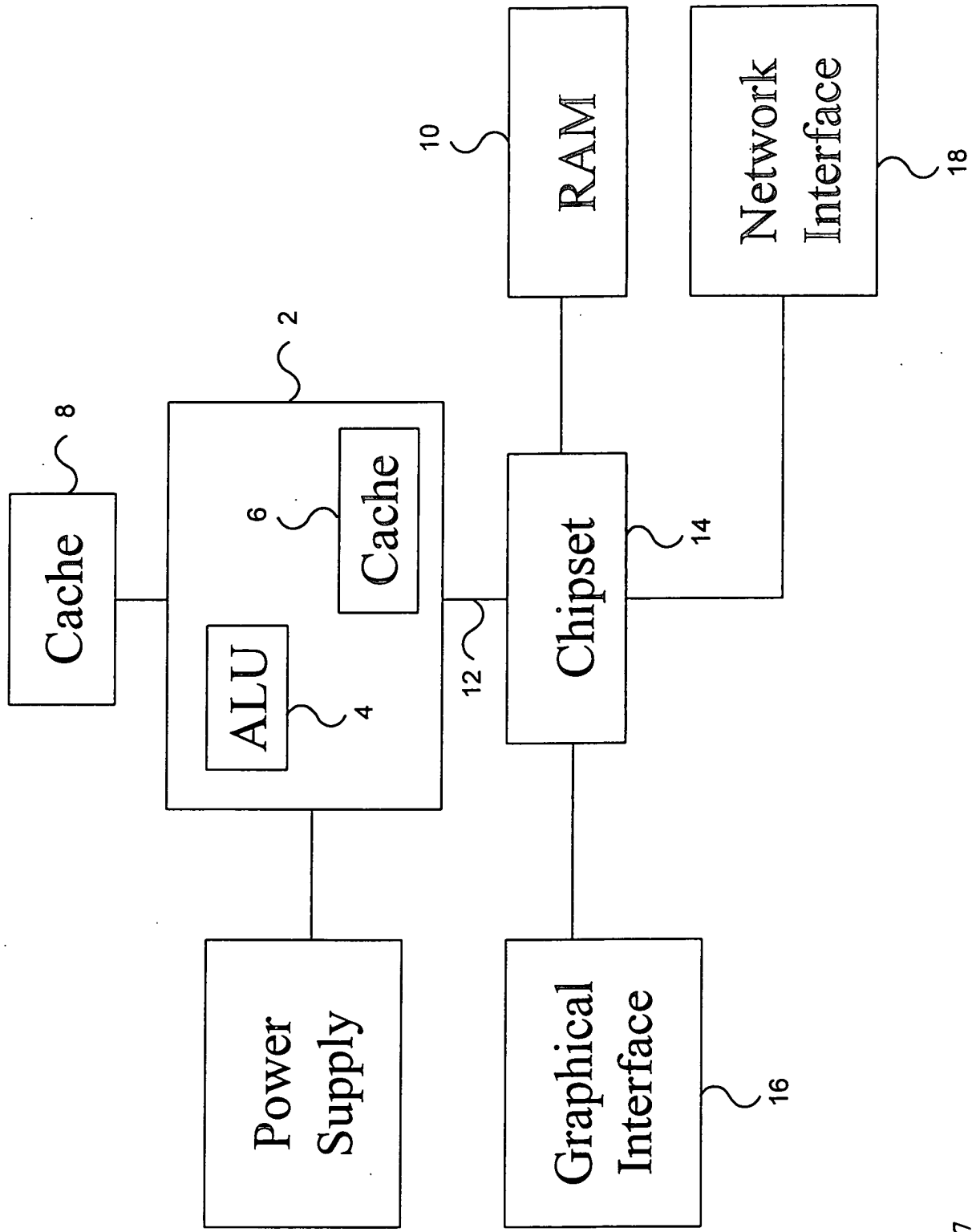


Figure 7